LG Display

LP173WD1
Liquid Crystal Display

Product Specification

SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**
(●) **Final Specification**

Title	17.3” HD+ TFT LCD

BUYER	
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP173WD1
Suffix	TLC2

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE
K. J. KWON / S.Manager	
REVIEWED BY	
G. J. Han / Manager	
PREPARED BY	
H. M. Yoon / Engineer H. J. Kim / Engineer	

Product Engineering Dept.
LG Display Co., Ltd

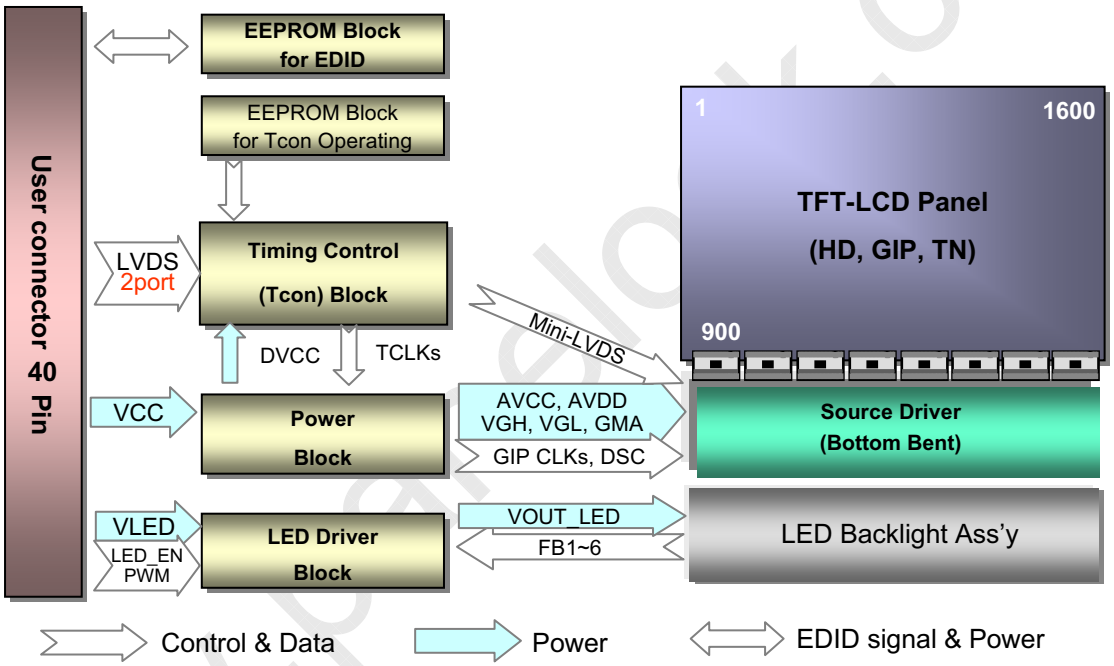
Contents

RECORD OF REVISIONS

Revision No	Revision Date	Page	Description	EDID ver
0.0	May. 01. 2009	-	First Draft	0.0
1.0	May. 27, 2009	-	Final CAS	1.0
1.1	May.30, 2009		Revision (TLC1→TLC2)	1.0

1. General Description

The LP173WD1 is a Color Active Matrix Liquid Crystal Display with an integral LED backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally white mode. This TFT-LCD has 17.3 inches diagonally measured active display area with WHD+ resolution(1600 horizontal by 900 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors. The LP173WD1 has been designed to apply the interface method that enables low power, high speed, low EMI. The LP173WD1 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP173WD1 characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	17.3 inches diagonal
Outline Dimension	398.1(H, Typ.) × 232.8(V, Typ.) × 6.0(D, Max.) mm
Pixel Pitch	0.23868 X 0.23868 mm
Pixel Format	1600 horiz. by 900 vert. Pixels RGB strip arrangement
Color Depth	6-bit, 262,144 colors
Luminance, White	200 cd/m^2(Typ., @I_{LED}=21mA)
Power Consumption	Logic : 1.5 W (Typ.@Mosaic), Back Light : 5.0W (Typ.)
Weight	570g (Max.)
Display Operating Mode	Transmissive mode, normally white
Surface Treatment	Glare treatment of the front Polarizer
RoHS Comply	Yes
BFR / PVC / As Free	Yes all.

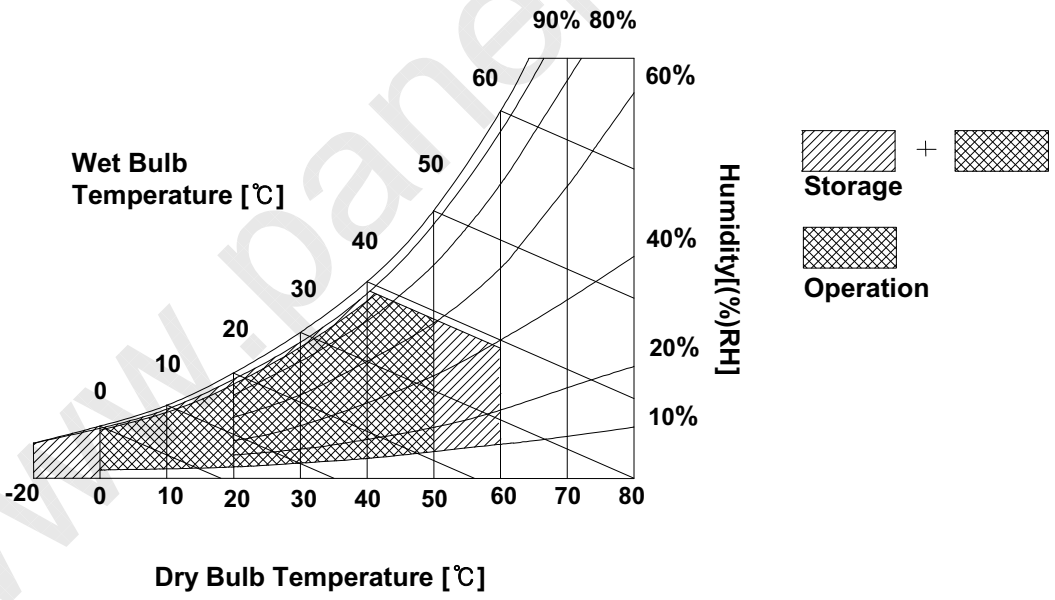
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	HST	-20	60	°C	1
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

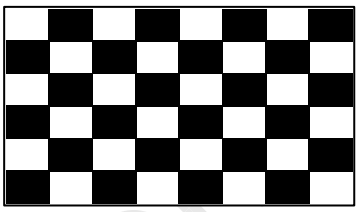
The LP173WD1 requires two power inputs. The first logic is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second backlight is the input about LED BL with LED Driver.

Table 2. ELECTRICAL CHARACTERISTICS

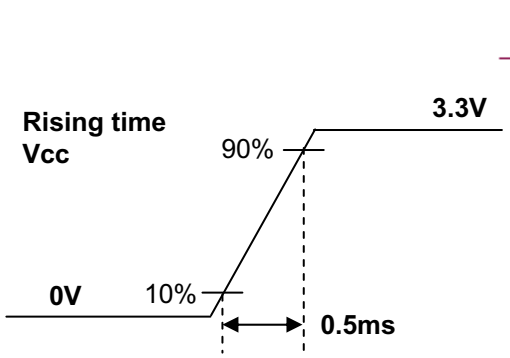
Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
LOGIC :							
Power Supply Input Voltage		V_{CC}	3.0	3.3	3.6	V	1
Power Supply Input Current	Mosaic	I_{CC}	-	455	515	mA	2
	Black	I_{CC_max}	-	575	660	mA	3
Power Consumption		P_{CC}	-	1.5	1.7	W	2
Power Supply Inrush Current		I_{CC_P}	-	1200	1800	mA	4
LVDS Impedance		Z_{LVDS}	90	100	110	Ω	5
BACKLIGHT : (with LED Driver)							
LED Power Input Voltage		V_{LED}	7.0	12.0	20.0	V	6
LED Power Input Current		I_{LED}	-	21	25	mA	7
LED Power Consumption		P_{LED}	-	5.0	5.3	W	7
LED Power Inrush Current		I_{LED_P}	-	800	1000	mA	8
PWM Duty Ratio			6	-	100	%	9
PWM Jitter		-	0	-	0.2	%	10
PWM Impedance		Z_{PWM}	20	40	60	kΩ	
PWM Frequency		F_{PWM}	200	-	1000	Hz	11
PWM High Level Voltage		V_{PWM_H}	3.0	-	5.3	V	
PWM Low Level Voltage		V_{PWM_L}	0	-	0.5	V	
LED_EN Impedance		Z_{PWM}	20	40	60	kΩ	
LED_EN High Voltage		$V_{LED\_EN\_H}$	3.0	-	5.3	V	
LED_EN Low Voltage		$V_{LED\_EN\_L}$	0	-	0.5	V	
Life Time			12,000	-	-	Hrs	12

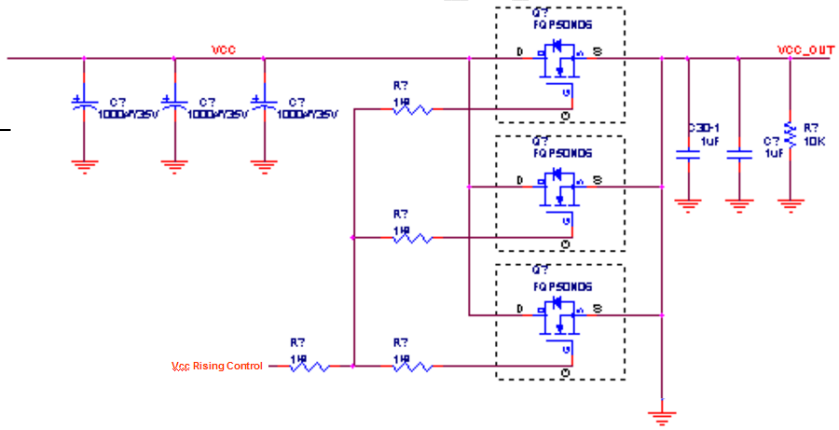
Note)

1. The measuring position is the connector of LCM and the test conditions are under 25℃, fv = 60Hz, Black pattern.
2. The specified Icc current and power consumption are under the Vcc = 3.3V , 25℃, fv = 60Hz condition whereas Mosaic pattern is displayed and fv is the frame frequency.

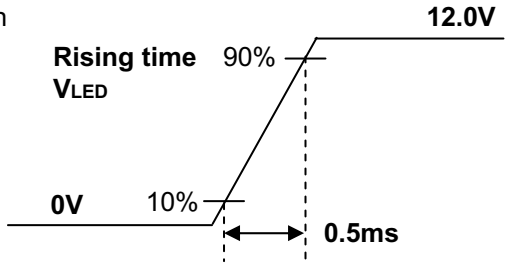


3. This Spec. is the max load condition for the cable impedance designing.
4. The below figures are the measuring Vcc condition and the Vcc control block LGD used. The Vcc condition is same the minimum of T1 at Power on sequence.





5. This impedance value is needed to proper display and measured form LVDS Tx to the mating connector.
6. The measuring position is the connector of LCM and the test conditions are under 25℃.
7. The current and power consumption with LED Driver are under the Vled = 12.0V , 25℃, Dimming of Max luminance whereas White pattern is displayed and fv is the frame frequency.
8. The below figures are the measuring Vled condition and the Vled control block LGD used. VLED control block is same with Vcc control block.



9. The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.
10. If Jitter of PWM is bigger than maximum. It may cause flickering.
11. This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
12. The life time is determined as the time at which the typical brightness of LCD is 50% compare to that of initial value at the typical LED current. These LED backlight has 6 strings on it and the typical current of LED's string is base on 21mA.

3-2. Interface Connections

This LCD employs two interface connections, a 40 pin connector is used for the module electronics interface and the other connector is used for the integral backlight system.

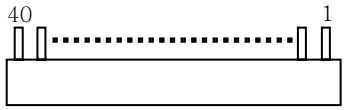
The electronics interface connector is a model CABLINE-VS RECE ASS'Y manufactured by I-PEX.

Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

Pin	Symbol	Description	Notes
1	NC	No Connection	
2	VCC	Power Supply, 3.3V Typ.	
3	VCC	Power Supply, 3.3V Typ.	
4	V EEDID	DDC 3.3V power	
5	NC	No Connection	
6	Clk EEDID	DDC Clock	
7	DATA EEDID	DDC Data	
8	Odd_R_{IN} 0-	Negative LVDS differential data input	
9	Odd_R_{IN} 0+	Positive LVDS differential data input	
10	GND	Ground	
11	Odd_R_{IN} 1-	Negative LVDS differential data input	
12	Odd_R_{IN} 1+	Positive LVDS differential data input	
13	GND	Ground	
14	Odd_R_{IN} 2-	Negative LVDS differential data input	
15	Odd_R_{IN} 2+	Positive LVDS differential data input	
16	GND	Ground	
17	Odd_CLKIN-	Negative LVDS differential clock input	
18	Odd_CLKIN+	Positive LVDS differential clock input	
19	GND	Ground	
20	Even_R_{IN} 0-	Negative LVDS differential data input (R0-R5,G0)	
21	Even_R_{IN} 0+	Positive LVDS differential data input (R0-R5,G0)	
19	GND	Ground	
23	Even_R_{IN} 1-	Negative LVDS differential data input (G1-G5,B0-B1)	
24	Even_R_{IN} 1+	Positive LVDS differential data input (G1-G5,B0-B1)	
19	GND	Ground	
26	Even_R_{IN} 2-	Negative LVDS differential data input (B2-B5,HS,VS,DE)	
27	Even_R_{IN} 2+	Positive LVDS differential data input (B2-B5,HS,VS,DE)	
19	GND	Ground	
29	Even_CLKIN-	Negative LVDS differential clock input	
30	Even_CLKIN+	Positive LVDS differential clock input	
31	GND	LED Ground	
32	GND	LED Ground	
33	GND	LED Ground	
34	NC	No Connection	
35	PWM	PWM for luminance control(200Hz ~ 1000Hz)	
36	LED_EN	Backlight On/Off Control	
37	NC	No Connection (Reserved)	
38	VLED	LED Power Supply (7V-21V)	
39	VLED	LED Power Supply (7V-21V)	
40	VLED	LED Power Supply (7V-21V)	

1, Interface chips
1.1 LCD : SW, SW0617 (LCD Controller) including LVDS Receiver
1.2 System : THC63LVDF823A or equivalent
* Pin to Pin compatible with LVDS

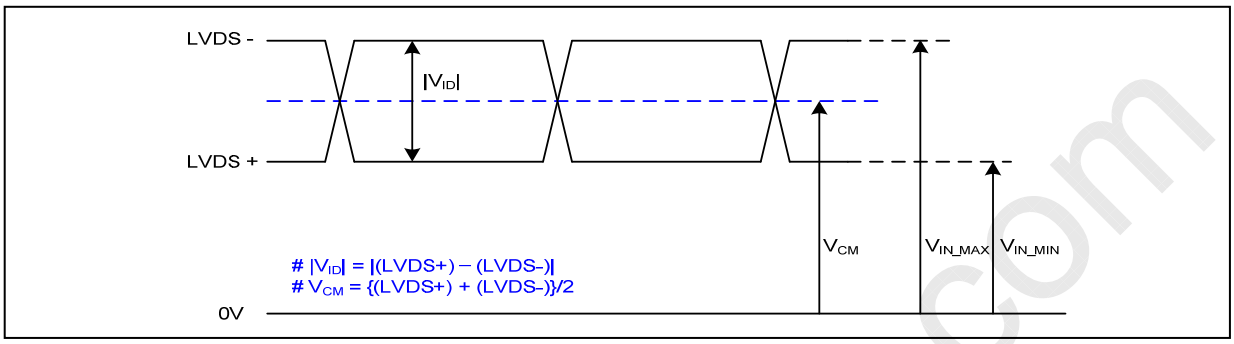
2. Connector
2.1 LCD : CABLINE-VS RECE ASS'Y, I-PEX or its compatibles
2.2 Mating : CABLINE-VS PLUG CABLE ASS'Y or equivalent.
2.3 Connector pin arrangement



[LCD Module Rear View]

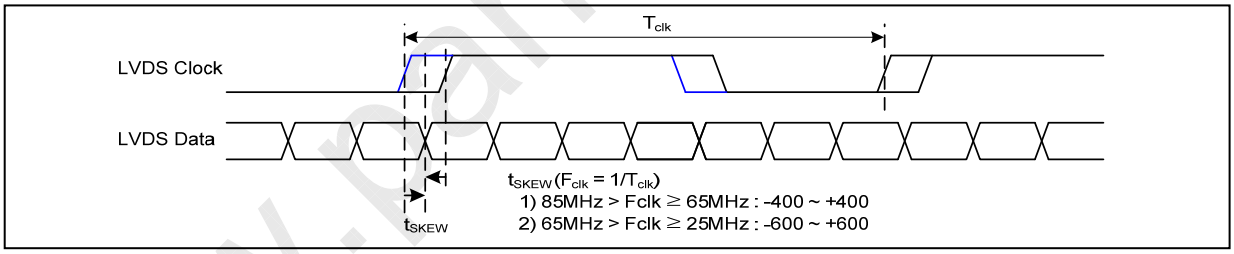
3-3. LVDS Signal Timing Specifications

3-3-1. DC Specification

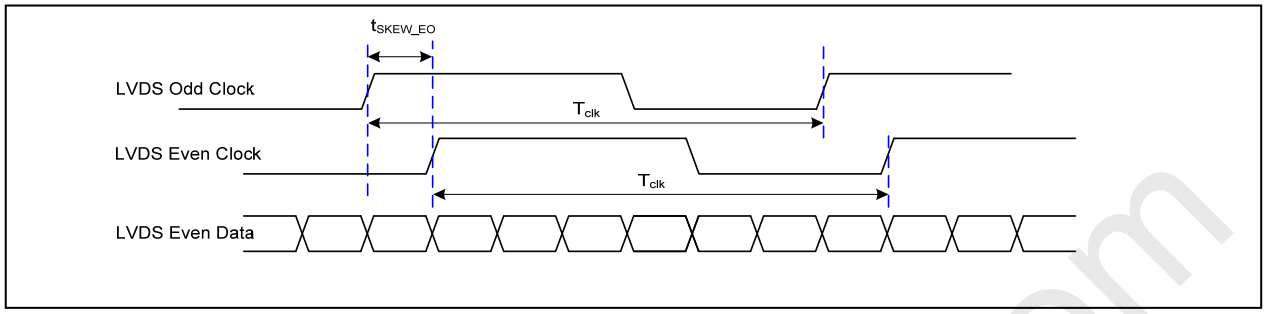


Description	Symbol	Min	Max	Unit	Notes
LVDS Differential Voltage	$\|V_{ID}\|$	100	600	mV	-
LVDS Common mode Voltage	V_{CM}	0.6	1.8	V	-
LVDS Input Voltage Range	V_{IN}	0.3	2.1	V	-

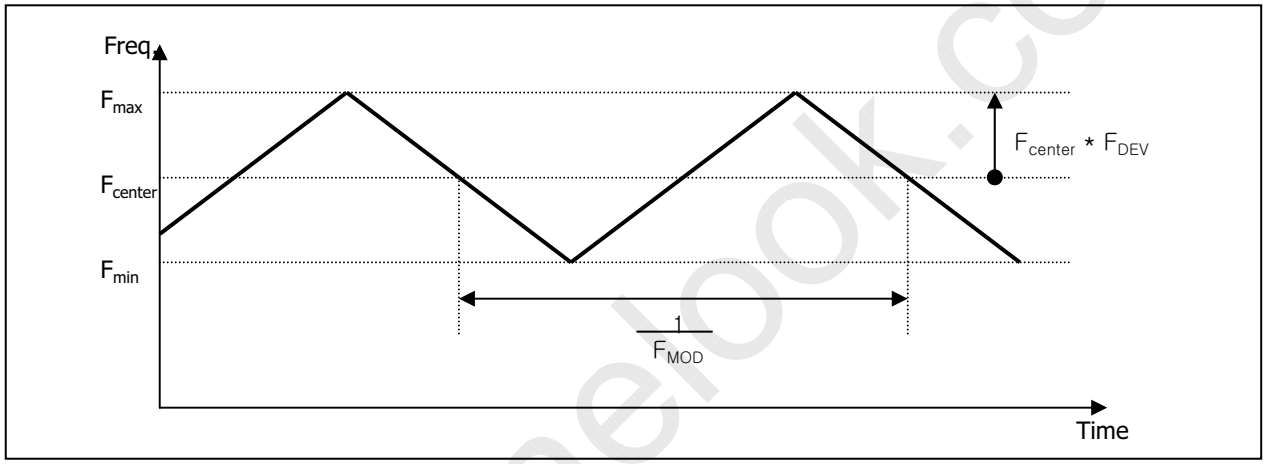
3-3-2. AC Specification



Description	Symbol	Min	Max	Unit	Notes
LVDS Clock to Data Skew Margin	t_{SKEW}	- 400	+ 400	ps	85MHz > Fclk ≥ 65MHz
	t_{SKEW}	- 600	+ 600	ps	65MHz > Fclk ≥ 25MHz
LVDS Clock to Clock Skew Margin (Even to Odd)	t_{SKEW_EO}	- 1/7	+ 1/7	T_{clk}	-
Maximum deviation of input clock frequency during SSC	F_{DEV}	-	± 3	%	-
Maximum modulation frequency of input clock during SSC	F_{MOD}	-	200	KHz	-



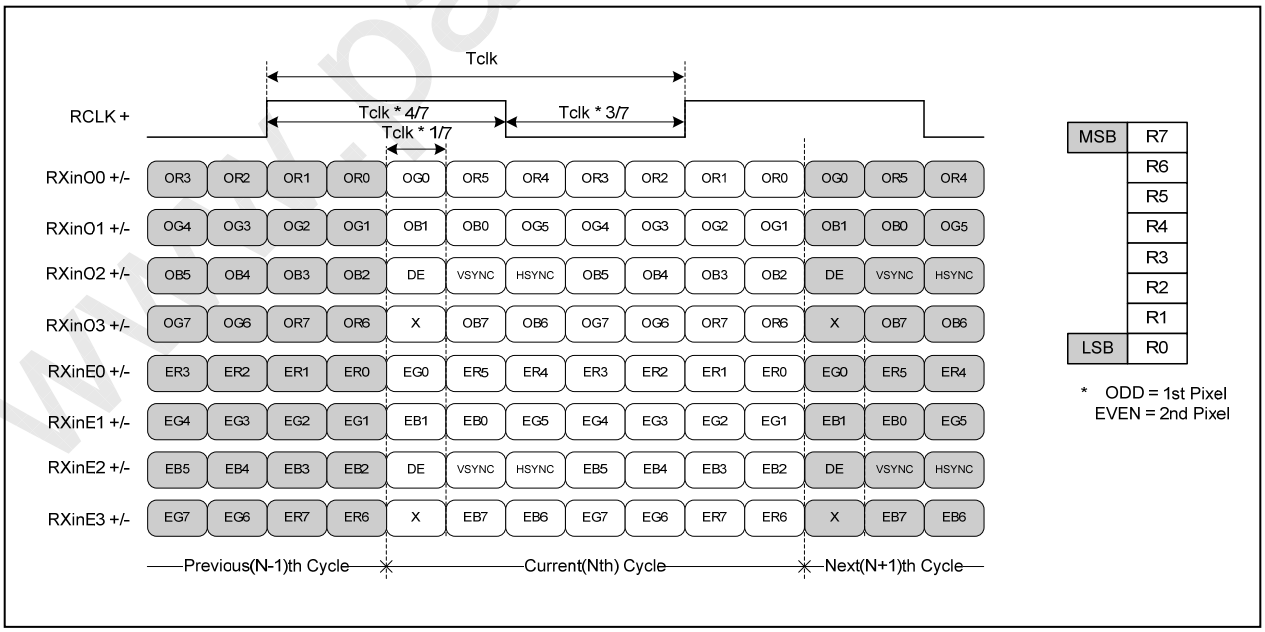
< Clock skew margin between channel >



< Spread Spectrum >

3-3-3. Data Format

1) LVDS 2 Port



< LVDS Data Format >

3-4. Signal Timing Specifications

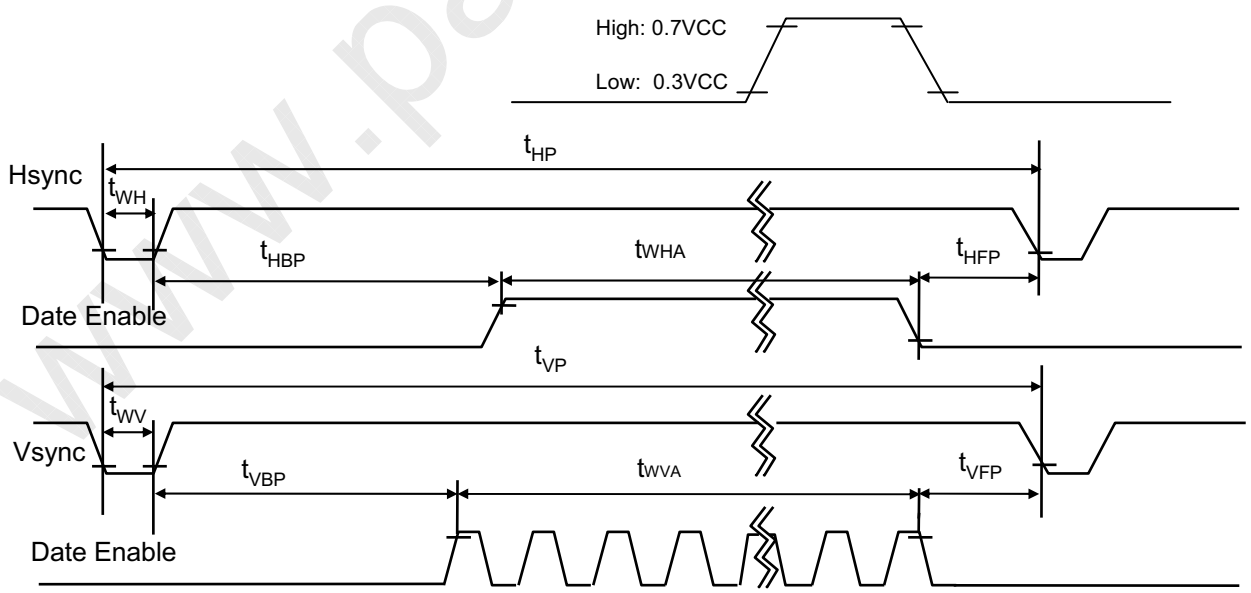
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of LVDS Tx/Rx for its proper operation.

Table 5. TIMING TABLE

ITEM	Symbol		Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	f_{CLK}	47.375	48.875	50.375	MHz	2 Port
Hsync	Period	t_{HP}	868	892	908	tCLK	2 Port
	Width	t_{WH}	20	24	32		
	Width-Active	tw_{HA}	800	800	800		
Vsync	Period	t_{VP}	907	912	926	tHP	
	Width	t_{WV}	2	3	5		
	Width-Active	tw_{VA}	900	900	900		
Data Enable	Horizontal back porch	t_{HBP}	32	44	48	tCLK	2 Port
	Horizontal front porch	t_{HFP}	16	24	28		
	Vertical back porch	t_{VBP}	4	7	15	tHP	
	Vertical front porch	t_{VFP}	1	2	6		

3-5. Signal Timing Waveforms

Condition : V_{CC} =3.3V



3-6. Color Input Data Reference

The brightness of each primary color (red,green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 6. COLOR DATA REFERENCE

Color		Input Color Data																	
		RED						GREEN						BLUE					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	…			…						…						…			
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	…			…						…						…			
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	…			…						…						…			
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

3-7. Power Sequence

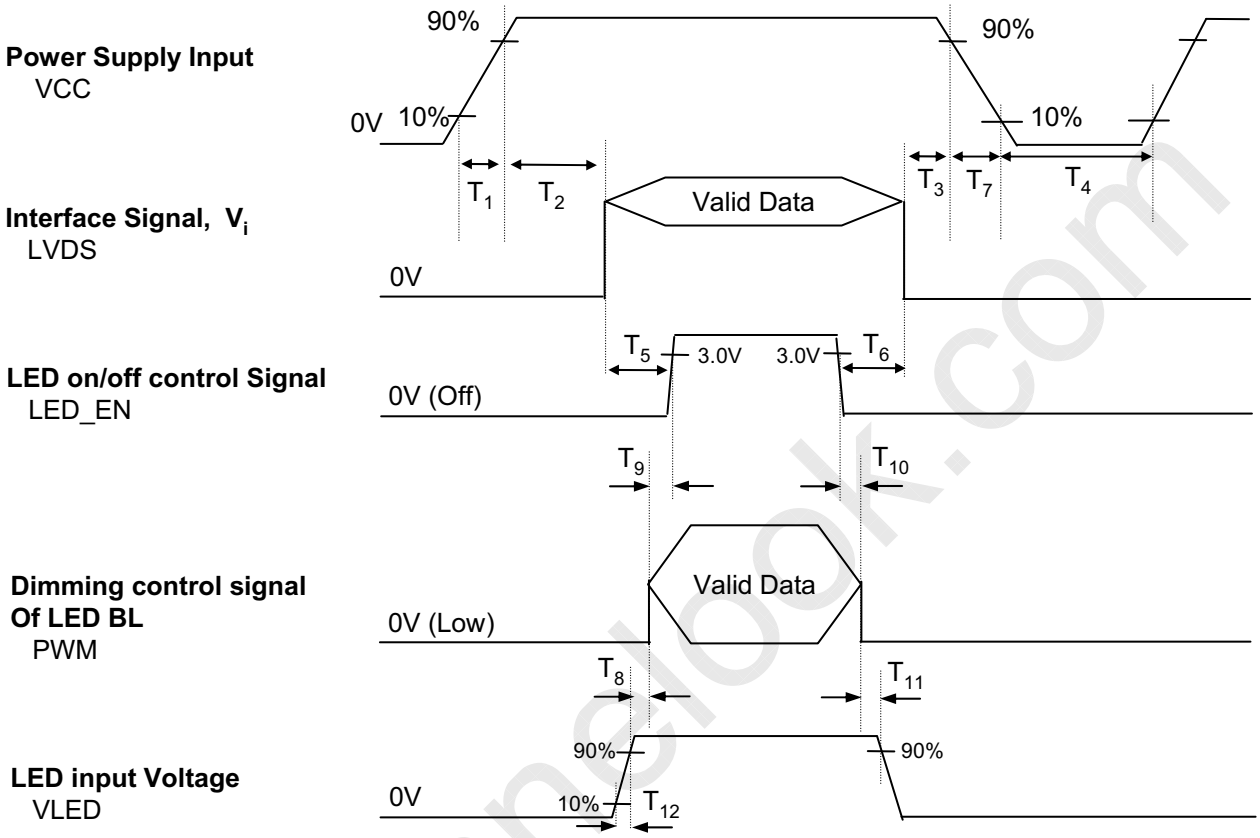


Table 6. POWER SEQUENCE TABLE

Logic Parameter	Value			Units	LED Parameter	Value			Units
	Min.	Typ.	Max.			Min.	Typ.	Max.	
T_1	0.5	-	10	ms	T_8	10	-	-	ms
T_2	0	-	50	ms	T_9	0	-	-	ms
T_3	0	-	50	ms	T_{10}	0	-	-	ms
T_4	400	-	-	ms	T_{11}	10	-	-	ms
T_5	200	-	-	ms	T_{12}	0.5	-	-	ms
T_6	200	-	-	ms					
T_7	3	-	10	ms					

Note)
1. Do not insert the mating cable when system turn on.
2. Valid Data have to meet "3-3. LVDS Signal Timing Specifications"
3. LVDS, LED_EN and PWM need to pull-down condition on invalid status.
4. LGD recommend the rising sequence of VLED after the Vcc and valid status of LVDS turn on.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

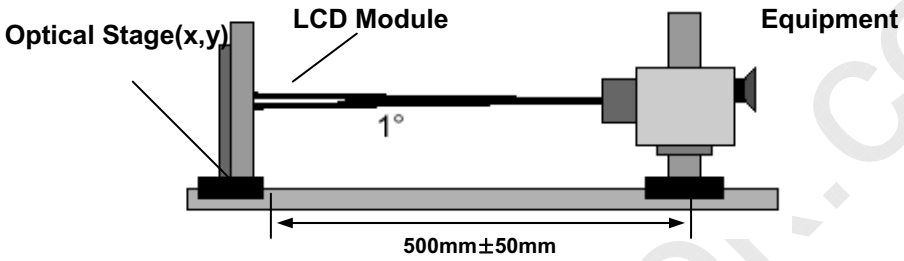


Table 8. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, f_{CLK}= 97.75MHz, ILED =21 mA

Parameter	Symbol	Values			Units	Notes
		Min	Typ	MAx		
Contrast Ratio	CR	500	600	-		1
Surface Luminance, white	L_{WH}	170	200	-	cd/m²	2
Luminance Variation	δ_{WHITE}		1.4	1.6		3
Response Time	$Tr_R + Tr_D$	-	8	16	ms	4
Color Coordinates						
RED	RX	0.586	0.616	0.646		
	RY	0.316	0.346	0.376		
GREEN	GX	0.285	0.315	0.345		
	GY	0.572	0.602	0.632		
BLUE	BX	0.122	0.152	0.182		
	BY	0.080	0.110	0.140		
WHITE	WX	0.283	0.313	0.343		
	WY	0.299	0.329	0.359		
Viewing Angle						5
x axis, right(Φ=0°)	Θr	40			degree	
x axis, left (Φ=180°)	Θl	40			degree	
y axis, up (Φ=90°)	Θu	10			degree	
y axis, down (Φ=270°)	Θd	30			degree	
Gray Scale	-	-				6

Note)

1. Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 1.

$$L_{WH} = \text{Average}(L_1, L_2, \ldots L_5)$$

3. The variation in surface luminance , The panel total variation (δ_{WHITE}) is determined by measuring L_N at each test position 1 through 13 and then defined as followed numerical formula. For more information see FIG 2.

$$\delta_{WHITE} = \frac{\text{Maximum}(L_1, L_2, \ldots L_{13})}{\text{Minimum}(L_1, L_2, \ldots L_{13})}$$

4. Response time is the time required for the display to transition from white to black (rise time, Tr_R) and from black to white(Decay Time, Tr_D). For additional information see FIG 3.

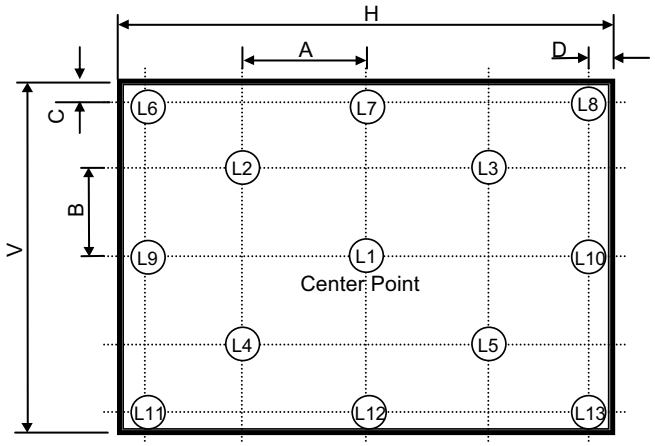
5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

6. Gray scale specification * f_V = 60Hz

Gray Level	Luminance [%] (Typ)
L0	0.0
L7	0.8
L15	4.25
L23	10.9
L31	21.0
L39	34.8
L47	52.5
L55	74.2
L63	100

FIG. 2 Luminance

<Measuring point for Average Luminance & measuring point for Luminance variation>



H,V : ACTIVE AREA
A : H/4 mm
B : V/4 mm
C : 10 mm
D : 10 mm
POINTS : 13 POINTS

FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

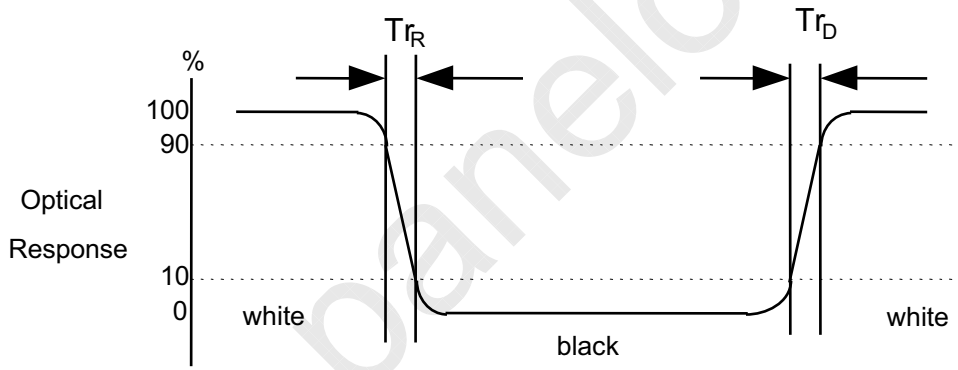
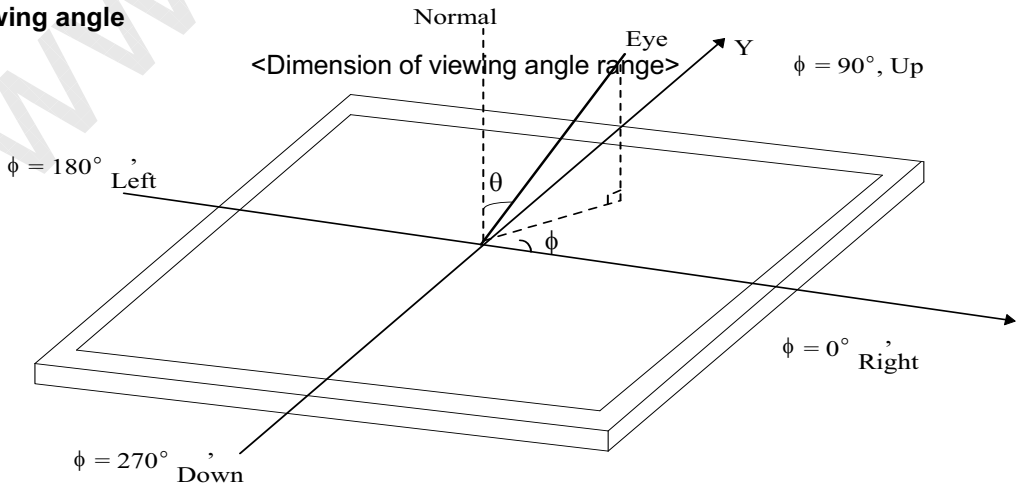


FIG. 4 Viewing angle



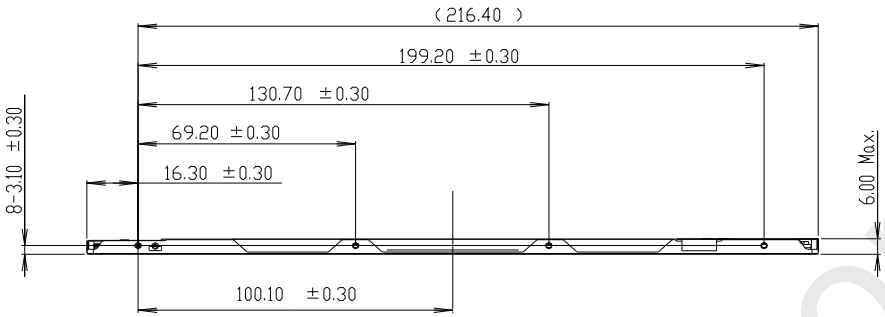
5. Mechanical Characteristics

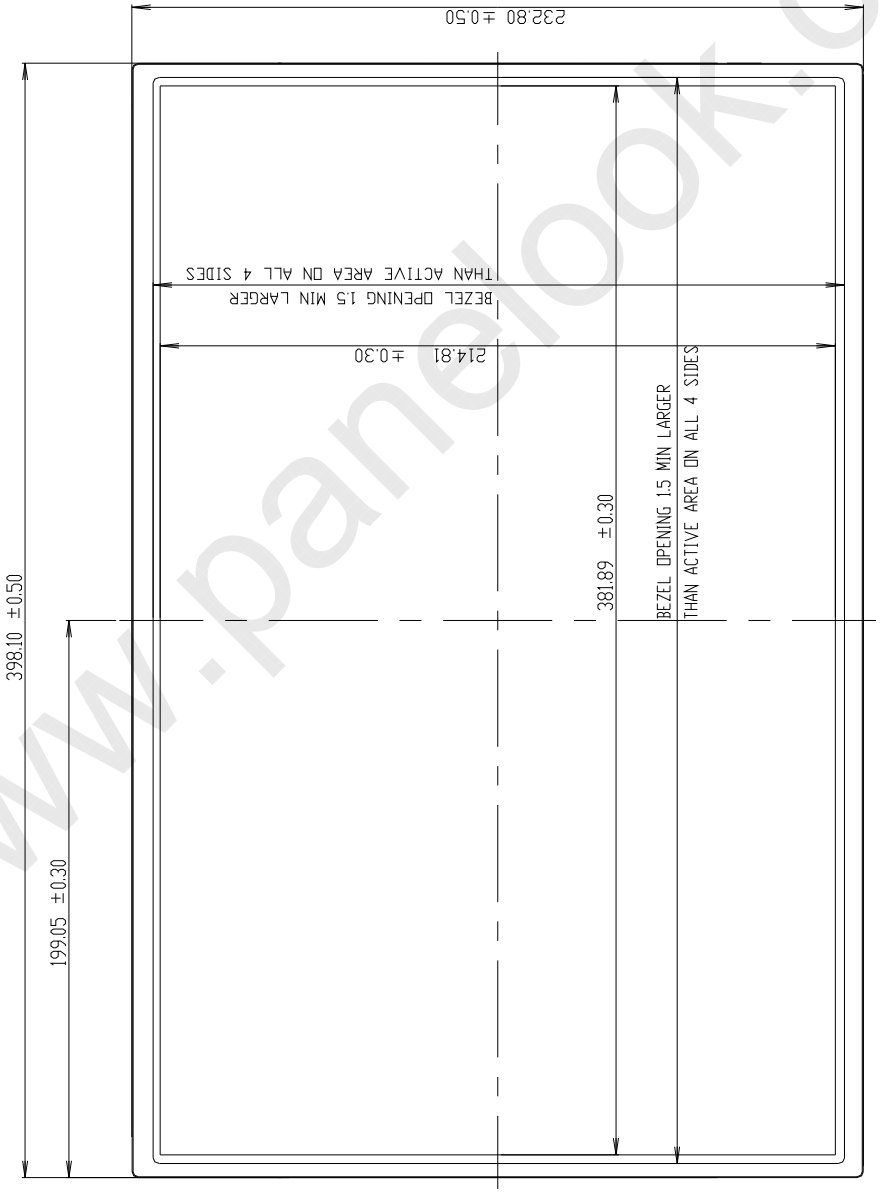
The contents provide general mechanical characteristics for the model LP173WD1.
In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	398.1 ± 0.50mm
	Vertical	232.8 ± 0.50mm
	Depth	6.0mm(Max.)
Bezel Area	Horizontal	1.5mm Min.(Lager than Active Display Area)
	Vertical	1.5mm Min.(Lager than Active Display Area)
Active Display Area	Horizontal	381.89mm
	Vertical	214.81 mm
Weight	570g (Max.)	
Surface Treatment	Glare treatment of the front Polarizer (Haze 0%)	

<FRONT VIEW>

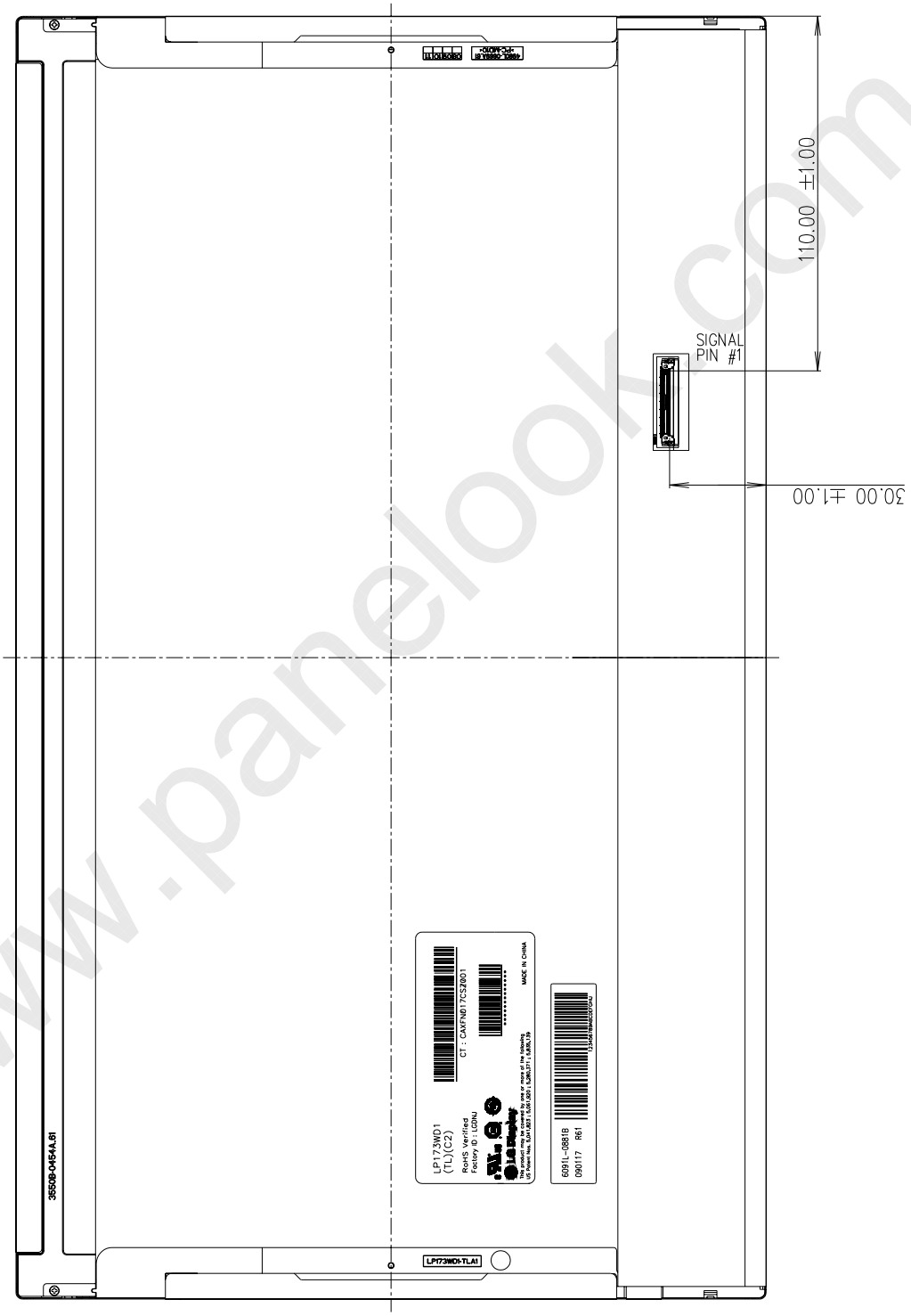
Note) Unit:[mm], General tolerance: ± 0.5mm



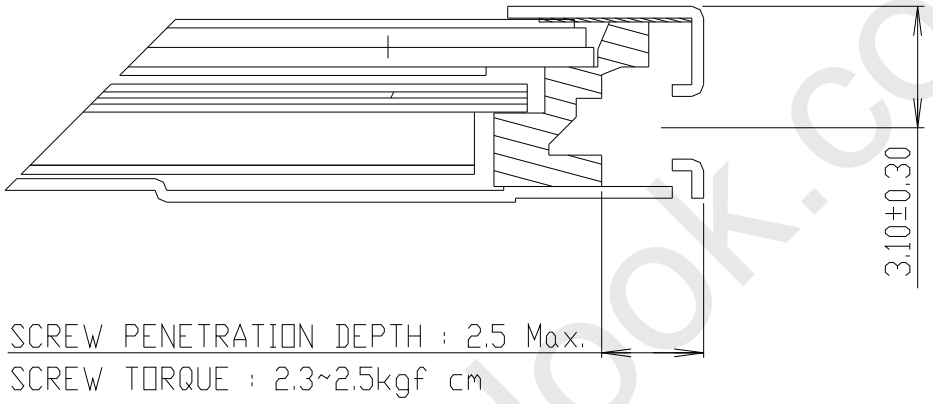


<REAR VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm

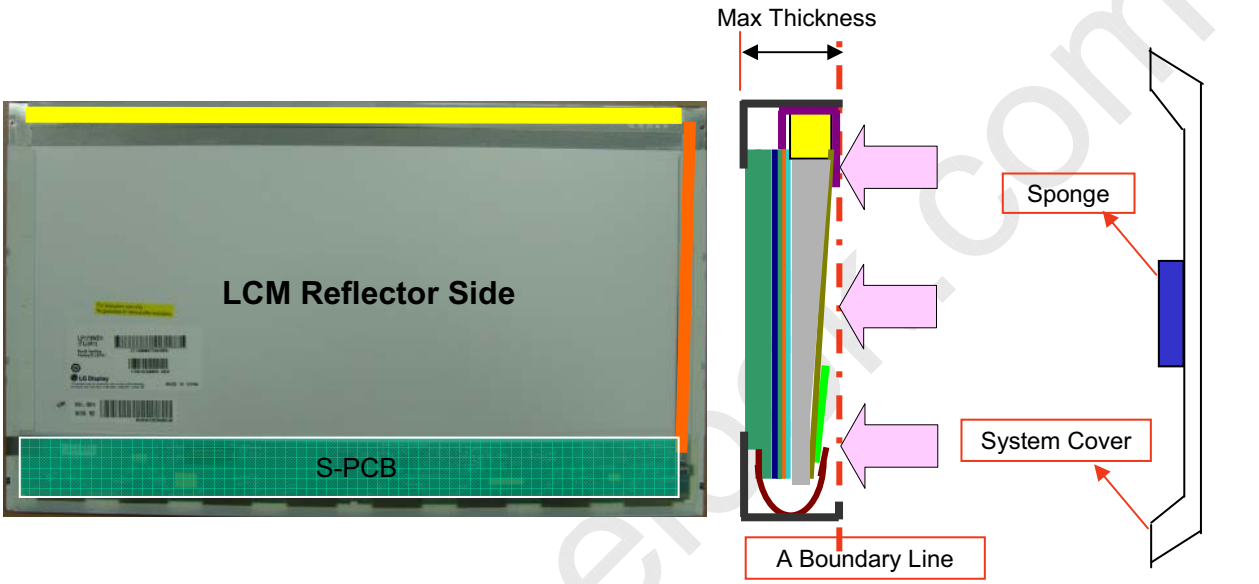


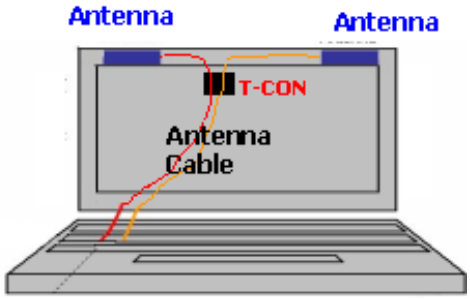
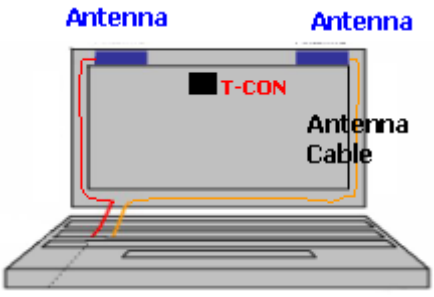
[DETAIL DESCRIPTION OF SIDE MOUNTING SCREW]



LGD Proposal for system cover design.(Appendix)

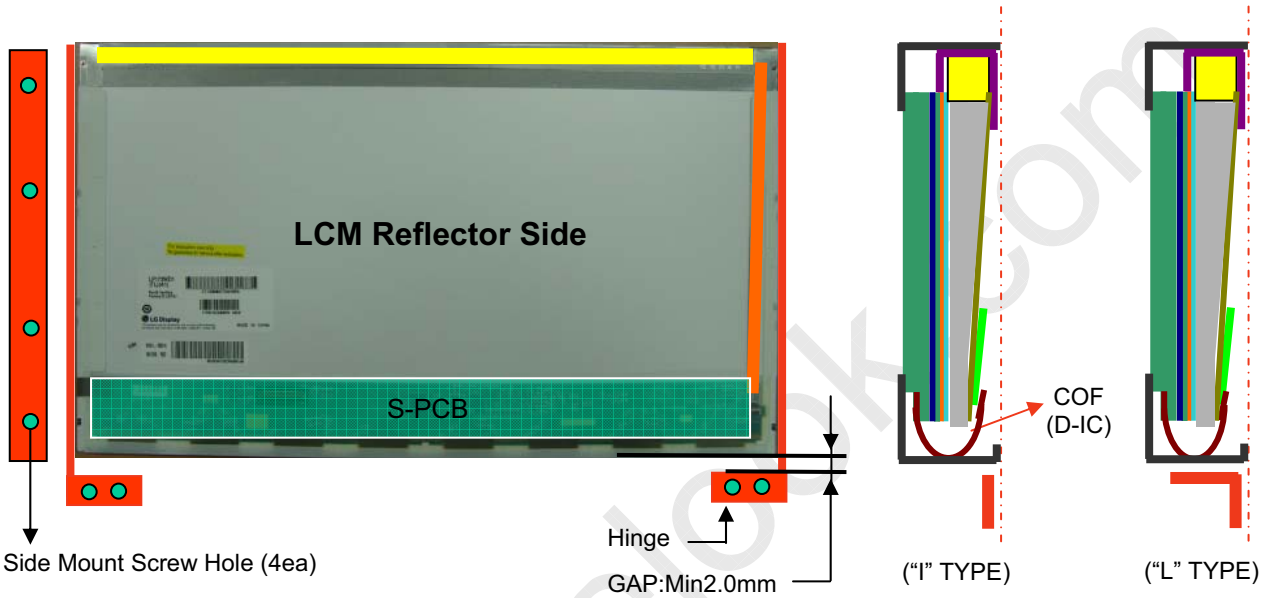
1	Gap check for securing the enough gap between LCM and System cover.	



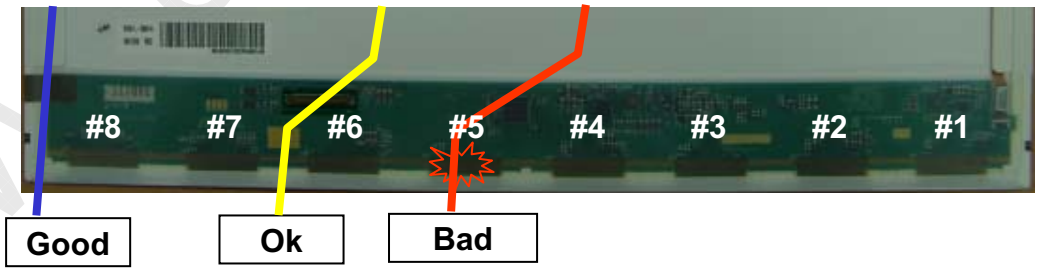
Define	1.Rear side of LCM is sensitive against external stress,and previous check about interference is highly needed. 2.In case there is something from system cover comes into the boundary above,mechanical interference may cause the FOS defects. (Eg:Ripple,White spot..)
2	Check if antenna cable is sufficiently apart from T-CON of LCD Module.
Define	 NO GOOD  GOOD
	1.If system antenna is overlapped with T-CON,it might be cause the noise.

LGD Proposal for system cover design.

3	Gap check for securing the enough gap between LCM and System hinge.	



Define	1.At least 2.0mm of gap needs to be secured to prevent the shock related defects. 2."L" type of hinge is recommended than "I" type under shock test.
4	Checking the path of the System wire.

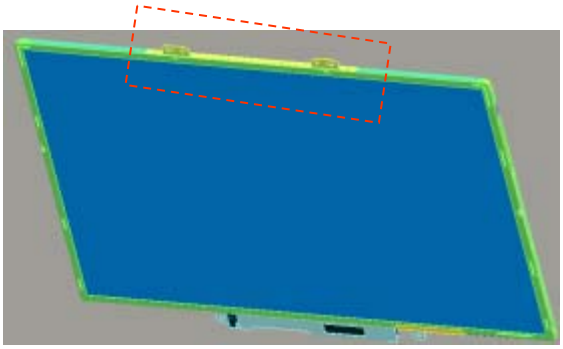


Define	1.COF area needs to be handled with care. 2.GOOD ➔Wire path design to system side. OK➔ Wire path is located between COFs. BAD➔Wire path overlapped with COF area.

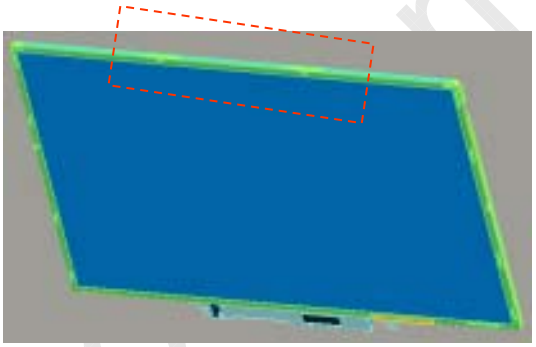
LGD Proposal for system cover design.

5	Using a bracket on the top of LCM is not recommended.	

bracket

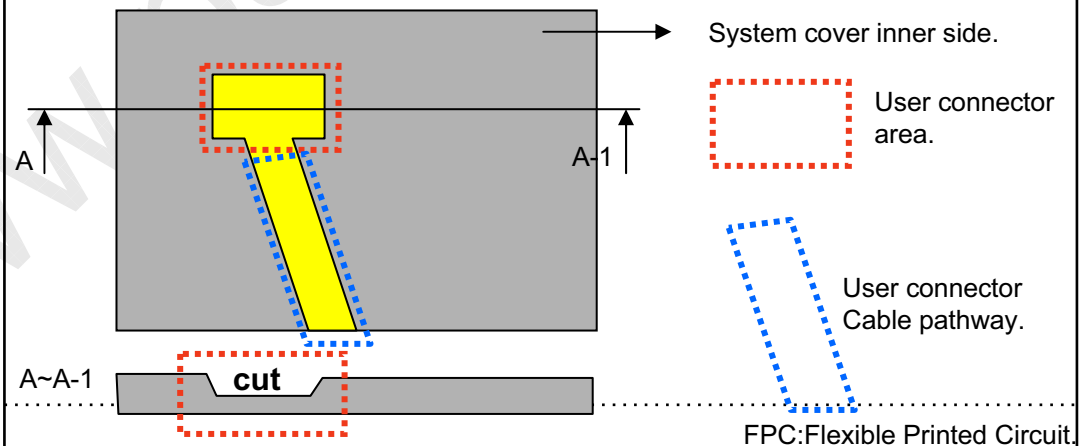


With bracket



Without bracket

Define	1.Condition without bracket is good for mechanical noise,and can minimize the light leakage from deformation of bracket. 2.The results shows that there is no difference between the condition with or without bracket.
6	Securing additional gap on CNT area..



Define	1.CNT area is specially sensitive against external stress,and additional gap by cutting on system cover will be helpful on removing the Ripple. 2.Using a thinner CNT will be better. (eg: FPC type)

6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Sine wave, 5 ~ 150Hz, 1.5G, 0.37oct/min 3 axis, 30min/axis
6	Shock test (non-operating)	Half sine wave, 180G, 2ms one shock of each six faces(I.e. run 180G 2ms for all six faces)
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr
8	Image Sticking [1)]	Ta= 25°C, Pattern : Mosaic(8 by 6), Operating Time : 30 min Lamp Operating Current : 6.0mA

{ Result Evaluation Criteria }
There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

1)

Mosaic Pattern(8 by 6) Half Gray

<Judgment Condition>
: Operating during 30 minutes with Mosaic Pattern(8 by 6), there is no Image Sticking after 10 second with half gray pattern.

7. International Standards

7-1. Safety

a) UL 60950-1:2003, First Edition, Underwriters Laboratories, Inc.,
Standard for Safety of Information Technology Equipment.
b) CAN/CSA C22.2, No. 60950-1-03 1st Ed. April 1, 2003, Canadian Standards Association,
Standard for Safety of Information Technology Equipment.
c) EN 60950-1:2001, First Edition,
European Committee for Electrotechnical Standardization(CENELEC)
European Standard for Safety of Information Technology Equipment.

7-2. EMC

a) ANSI C63.4 “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHZ to 40GHz. “American National Standards Institute(ANSI), 1992
b) CISPR22 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ International Special Committee on Radio Interference.
c) EN 55022 “Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment.“ European Committee for Electrotechnical Standardization.(CENELEC), 1998
(Including A1: 2000)

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
Mark	1	2	3	4	5	6	7	8	9	0

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 20pcs

b) Box Size :490X390X298

9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 1/3

LP173WD1-TLC2 E-EDID DATA (ver0.0)

2009-04-.23

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)		Value (binary)	
0	00	Header	0	0	0000 0000	Header
1	01		F	F	1111 1111	
2	02		F	F	1111 1111	
3	03		F	F	1111 1111	
4	04		F	F	1111 1111	
5	05		F	F	1111 1111	
6	06		F	F	1111 1111	
7	07		0	0	0000 0000	
8	08	EISA manufacturer code = LGD	3	0	0011 0000	Vender/ Product ID
9	09		E	4	1110 0100	
10	0A	Product code = 0226	2	6	0010 0110	
11	0B	(Hex, LSB first)	0	2	0000 0010	
12	0C	32-bit serial number	0	0	0000 0000	
13	0D		0	0	0000 0000	
14	0E		0	0	0000 0000	
15	0F		0	0	0000 0000	
16	10	Week of manufacture	0	0	0000 0000	
17	11	Year of manufacture = 2009	1	3	0001 0011	
18	12	EDID Structure version # = 1	0	1	0000 0001	EDID Version/ Revision
19	13	EDID Revision # = 3	0	3	0000 0011	
20	14	Video input definition = Digital I/p,non TMDS CRGB	8	0	1000 0000	Display Parameter
21	15	Max H image size(㎝) = 38,208㎝(38)	2	6	0010 0110	
22	16	Max V image size(㎝) = 21,492㎝(21)	1	5	0001 0101	
23	17	Display gamma = 2.20	7	8	0111 1000	
24	18	Feature support(DPMS) = Active off, RGB Color	0	A	0000 1010	
25	19	Red/Green low Bits	A	8	1010 1000	Color Characteristic
26	1A	Blue/White Low Bits	C	0	1100 0000	
27	1B	Red X Rx = 0.616	9	D	1001 1101	
28	1C	Red Y Ry = 0.346	5	8	0101 1000	
29	1D	Green X Gx = 0.315	5	0	0101 0000	
30	1E	Green Y Gy = 0.602	9	A	1001 1010	
31	1F	Blue X Bx = 0.152	2	6	0010 0110	
32	20	Blue Y By = 0.110	1	C	0001 1100	
33	21	White X Wx = 0.313	5	0	0101 0000	
34	22	White Y Wy = 0.329	5	4	0101 0100	
35	23	Established Timing I	0	0	0000 0000	Established Timings
36	24	Established Timing II	0	0	0000 0000	
37	25	Manufacturer's Timings	0	0	0000 0000	
38	26	Standard Timing Identification 1 was not used	0	1	0000 0001	Standard Timing ID
39	27	Standard Timing Identification 1 was not used	0	1	0000 0001	
40	28	Standard Timing Identification 2 was not used	0	1	0000 0001	
41	29	Standard Timing Identification 2 was not used	0	1	0000 0001	
42	2A	Standard Timing Identification 3 was not used	0	1	0000 0001	
43	2B	Standard Timing Identification 3 was not used	0	1	0000 0001	
44	2C	Standard Timing Identification 4 was not used	0	1	0000 0001	
45	2D	Standard Timing Identification 4 was not used	0	1	0000 0001	
46	2E	Standard Timing Identification 5 was not used	0	1	0000 0001	
47	2F	Standard Timing Identification 5 was not used	0	1	0000 0001	
48	30	Standard Timing Identification 6 was not used	0	1	0000 0001	
49	31	Standard Timing Identification 6 was not used	0	1	0000 0001	
50	32	Standard Timing Identification 7 was not used	0	1	0000 0001	
51	33	Standard Timing Identification 7 was not used	0	1	0000 0001	
52	34	Standard Timing Identification 8 was not used	0	1	0000 0001	
53	35	Standard Timing Identification 8 was not used	0	1	0000 0001	

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 2/3

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)		Value (binary)	
54	36	1600 X 900 @ 60Hz mode : pixel clock = 97.75MHz	2	F	0010 1111	Timing Descriptor #1
55	37	(Stored LSB first)	2	6	0010 0110	
56	38	Horizontal Active = 1600 pixels	4	0	0100 0000	
57	39	Horizontal Blanking = 184 pixels	B	8	1011 1000	
58	3A	Horizontal Active : Horizontal Blanking = 1600 : 184	6	0	0110 0000	
59	3B	Vertical Avtive = 900 lines	8	4	1000 0100	
60	3C	Vertical Blanking = 12 lines	0	C	0000 1100	
61	3D	Vertical Active : Vertical Blanking = 900 : 12	3	0	0011 0000	
62	3E	Horizontal Sync. Offset = 48 pixels	3	0	0011 0000	
63	3F	Horizontal Sync Pulse Width = 48 pixels	3	0	0011 0000	
64	40	Vertical Sync Offset = 2 lines, Sync Width = 3 lines	2	3	0010 0011	
65	41	Horizontal Vertical Sync Offset/Width upper 2bits = 0	0	0	0000 0000	
66	42	Horizontal Image Size = 382.08㎜(382)	7	E	0111 1110	
67	43	Vertical Image Size = 214.92㎜(215)	D	7	1101 0111	
68	44	Horizontal & Vertical Image Size	1	0	0001 0000	
69	45	Horizontal Border = 0	0	0	0000 0000	
70	46	Vertical Border = 0	0	0	0000 0000	
71	47	Non-interlaced,Normal display,no stereo,Digital separate sync,H/V pol negatives	1	9	0001 1001	
72	48	Detailed Timing Descriptor #2	0	0	0000 0000	Detailed Timing Description #2
73	49		0	0	0000 0000	
74	4A		0	0	0000 0000	
75	4B		0	0	0000 0000	
76	4C		0	0	0000 0000	
77	4D		0	0	0000 0000	
78	4E		0	0	0000 0000	
79	4F		0	0	0000 0000	
80	50		0	0	0000 0000	
81	51		0	0	0000 0000	
82	52		0	0	0000 0000	
83	53		0	0	0000 0000	
84	55		0	0	0000 0000	
85	55		0	0	0000 0000	
86	56		0	0	0000 0000	
87	57		0	0	0000 0000	
88	58		0	0	0000 0000	
89	59		0	0	0000 0000	
90	5A	Detailed Timing Descriptor #3	0	0	0000 0000	Detailed Timing Description #3
91	5B		0	0	0000 0000	
92	5C		0	0	0000 0000	
93	5D		F	E	1111 1110	
94	5E		0	0	0000 0000	
95	5F		0	0	0000 0000	
96	60		0	0	0000 0000	
97	61		0	0	0000 0000	
98	62	L	4	C	0100 1100	
99	63	G	4	7	0100 0111	
100	64	D	4	4	0100 0100	
101	65	i	6	9	0110 1001	
102	66	s	7	3	0111 0011	
103	67	p	7	0	0111 0000	
104	68	l	6	C	0110 1100	
105	69	a	6	1	0110 0001	
106	6A	y	7	9	0111 1001	
107	6B	LF	0	A	0000 1010	

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 3/3

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)	Value (binary)	
108	6C	Detailed Timing Descriptor #4	0 0	0000 0000	Detailed Timing Description #4
109	6D		0 0	0000 0000	
110	6E		0 0	0000 0000	
111	6F		F E	1111 1110	
112	70		0 0	0000 0000	
113	71	L	4 C	0100 1100	
114	72	P	5 0	0101 0000	
115	73	1	3 1	0011 0001	
116	74	7	3 7	0011 0111	
117	75	3	3 3	0011 0011	
118	76	W	5 7	0101 0111	
119	77	D	4 4	0100 0100	
120	78	1	3 1	0011 0001	
121	79	-	2 D	0010 1101	
122	7A	T	5 4	0101 0100	
123	7B	L	4 C	0100 1100	
124	7C	C	4 3	0100 0011	
125	7D	2	3 2	0011 0010	
126	7E	Extension flag = 00	0 0	0000 0000	Extension Flag
127	7F	Checksum	1 7	0001 0111	Checksum